Claims

What is claimed is:

1. A multibank DRAM macro, said macro comprising:

(a) a plurality of DRAM memory banks, each bank respectively comprising:

(i) an array of DRAM memory cells,

(ii) bitlines and wordlines, respectively defining columns and rows of the array,

(iii) a row address decoder circuit,

(iv) a column address decoder circuit,

(v) spare rows and columns for redundancy,

(b) a bank select input for each respective bank, each bank input controlling operation of its respective bank, and

(c) a data path receiver / driver shared by at least two banks.

2. The DRAM macro of claim 1 further comprising (d) a master select input.

3. The DRAM macro of claim 2 wherein said bank select inputs are latched to a falling edge of a signal from said master select input.

4. The DRAM macro of claim 1 wherein said macro further comprises a write enable input.

5. The DRAM macro of claim 1 wherein said macro further comprises a page mode select input.

6. The DRAM macro of claim 1 wherein each bank further comprises (vi) at least one sense amplifier.

7. The DRAM macro of claim 1 wherein each bank has capacity for about 1 Mb of data.

8. The DRAM macro of claim 7 wherein said macro comprises at least 4 of said banks.

9. An integrated circuit device comprising a logic core and a DRAM macro wherein said DRAM macro is a multibank DRAM macro comprising:

(a) a plurality of DRAM memory banks, each bank respectively comprising:
  (i) an array of DRAM memory cells,
  (ii) bitlines and wordlines, respectively defining columns and rows of the array,
  (iii) a row address decoder circuit,
  (iv) a column address decoder circuit ,
  (v) spare rows and columns for redundancy,

(b) a bank select input for each respective bank, each bank input controlling operation of its respective bank, and

(c) a data path receiver / driver shared by at least two banks.

10. The integrated circuit device of claim 9 wherein said DRAM macro further comprises (d) a master select input.

11. The integrated circuit device of claim 10 wherein said bank select inputs are latched to a falling edge of a signal from said master select input.

12. The integrated circuit device of claim 9 wherein said DRAM macro further comprises a write enable input.

13. The integrated circuit device of claim 9 wherein said DRAM macro further comprises a page mode select input.

14. The integrated circuit device of claim 9 wherein each bank of said DRAM macro further comprises (vi) at least one sense amplifier.

15. The integrated circuit device of claim 9 wherein each bank of said DRAM macro has capacity for about 1 Mb of data.

16. The integrated circuit device of claim 15 wherein said DRAM macro comprises at least 4 of said banks.